Remarks

The present application was filed on February 28, 2002. This is responsive to the Office Action mailed January 21, 2005 which finally rejected claims 1-27. No claims are amended herein. Reconsideration and withdrawal of the final rejection is respectfully requested to provide the prosecution on the merits that the Applicant is entitled to without having to appeal to force review of the present status.

Response to Arguments

It is the Examiner's burden to substantiate rejections by a preponderance of the evidence. *Ex parte Hanson*, 16 USPQ2d 1441, 1442-43 (Bd. Pat. App. & Int'f 1989); *In re Caveney*, 226 USPQ 1 (Fed. Cir. 1985). The Examiner has failed to meet that burden because the response to Applicant's argument is, as a whole, partially irrelevant, partially a misplaced reading of the cited reference, and partially incomprehensible.

1. The Examiner restates a first portion of Applicant's argument in the Response filed November 16, 2004:

> The Applicant contends, "The Applicant expressly traverses the Examiner's following assertion in the Office Action: Schachner teaches a reference signal is selected as an input sequence for comparing with readback (output) data to track errors...This statement overreachingly reads the claimed comparison of the input sequence and output sequence of claim 1 onto Schachner 730's comparison of an input signal to an input reference value."

The Examiner's rebuttal is broken down in parts A-D for clarity sake in the following:

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Part A

The Examiner disagrees and asserts that col. 21 lines 38-41 of Schachner explicitly teach that the first NRZ data input becomes the reference data

The Applicant agrees to the extent that the cited passage states that the NRZ data input can be the reference data: "If the NRZ data input at 1402 is the first input data, and is to become the reference data, then the NRZ data is fed...." (Schachner col. 21, lines 38-39, emphasis added) However, this statement is irrelevant in relation to Applicant's argument that Schachner does not disclose comparing input and output sequences as claimed.

Part B

(Note: the Abstract in Schachner teaches that an input signal is a signal stored the [sic] recording medium hence the NRZ data input at 1402 in Figure 14 of Schachner is input data.)

The Applicant agrees that the NRZ data input is an input signal. This is consistent with the Applicant's earlier argument that Schachner 730's comparison of an input signal to an input reference value does not anticipate the claimed comparison of the input sequence and output sequence. This statement is irrelevant in relation to Applicant's argument that Schachner does not disclose comparing input and output sequences as claimed.

Part C

Why would anyone expect the input to have similar values to the reference value, if some other signal different from the reference value was stored on the recording medium?

The Applicant can only conclude that this statement is incomprehensible. The Examiner has not met the burden of completeness in all matters. (35 U.S.C. 132; 37 C.F.R. 1.104; MPEP 707.07)

Part D

> The Examiner asserts that in a noiseless channel the stored input signal would be identical to the reference signal since the reference signal is substantially the input signal prior to being stored on the recording medium, which Schachner explicitly confirms in col. 21 lines 38-41 of Schachner.

The Examiner must provide an evidenciary basis for the rejection. *In re Zurko*, 59 USPQ2d 1693 (Fed. Cir. 2001). Here, the Examiner contrarily combines facts only within the Examiner's personal knowledge with extrapolating the disclosure of Schachner to improperly concoct an alleged disclosure related to a comparison of the first NRZ data input signal with the reference signal made from the first NRZ data input signal. This assertion is misplaced because Schachner is wholly silent, contrary to the Examiner's assertion, regarding receiving a particular NRZ data input signal, storing the particular NRZ data input signal as a reference signal, and then comparing the particular NRZ data input signal to the reference signal. What Schachner does in fact explicitly disclose is comparing NRZ data to a reference stored in memory (Schachner col. 22, lines 14-16). The reference can be selected as being the first NRZ data input (Schachner col. 22, lines 38-40). However, Schachner clearly contemplates that whether the NRZ data input can be used as the reference or can be used to compare to the reference, but that the alternative options are mutually exclusive:

> If the NRZ data input at 1402 is the first input data, and is to become the reference data, then the NRZ data is fed to NRZ memory 1428 and to data comparator 1414 from data buffer 1410, under the control of probe interface 1436. As data

comparator 1414 reads the input NRZ data, a marker bit is added to the data stream at the start of each data portion (read gate true signal) to indicate the beginning thereof. Thus, when this NRZ data with marker bit is received by NRZ memory 1428, it can be properly stored in a predetermined format, and can then be transferred to reference memory 1422 under the control of read/write control 1420 and address register 1426 in order to be stored as reference data. In addition the NRZ data and marker bit, reference memory 1422 also stores for each data portion (read gate true section) the number of data to be tested in the read gate true section.

If, however, the input NRZ data being forwarded from data buffer 1410 is new NRZ data to be compared to reference data, then the data is forwarded to data comparator 1414 as well as to NRZ memory 1428. The incoming NRZ data and reference data is clocked into data comparator 1414 by the gate, clock and index signals 1411, 1412 and 1413. When gate signal 1411 indicated that a read gate has gone true, data comparator 1414 checks the incoming data signal to determine the beginning of the data to be analyzed, as noted above. Once the beginning of the data section to be analyzed is found, a first data flag 1415 is transmitted to maximum size register 1416, size register 1418 and minimum size register 1424, which are all reset in response thereto.

Data comparator 1414 is then ready to compare the input NRZ data to the reference signal to determine if a mismatch occurs (see FIG. 12). Thus, the apparatus loads the reference signal from reference memory 1422. The size information indicating the size of the data section to be analyzed is forwarded on size value line 1414 to size register 1418. This size value indicates to read/write control 1422 the amount of data that will be read out from reference memory 1422 during this read gate true data section. During this read out, maximum size register confirms that the data to be read out is not greater than a maximum size which is to be analyzed by the apparatus, and minimum size register 1424 confirms that the size of the data is not less than a predetermined ID size (noted above).

Thereafter, each data bit is read from reference memory 1422 under control of read/write control 1420, and is compared to the incoming NRZ data. If an error is encountered, indicated by a difference between the reference data and the NRZ data, and error flag is fed to trigger control 1430 indicating that an error has occurred within the analyzed segment. Additionally,

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> an error indication bit indicates the precise location within the segment where an error is found. Trigger control 1430, through trigger buffer 1432, then outputs a trigger signal 1434 informing probe interface 1436 to find the portion of the analog head signal corresponding to the location of the data mismatch. This portion of the analog signal is then displayed on the display portion of the apparatus.
> (Schachner col. 21 line 38 to col. 22 line 27)

Furthermore, the Examiner's assumption that an input signal would be identical to a reference signal made from the input signal fits squarely within the prior solutions that resulted in the problems solved by the embodiments of the present invention. The Examiner's assertion is therefore also irrelevant because in the embodiments of the present invention the input and output sequences are not always identical, due in part to data transfer errors.

As for the Examiner's assertion that the input signal and the reference signal made from the input signal would be identical, this is not supported by the disclosure of Schachner and is therefore facts only within the personal knowledge of the Examiner. In accordance with 37 CFR 1.104(d)(2) the Applicant requests that the Examiner provide an affidavit specifically substantiating the reference.

2. The Examiner then restates a second portion of Applicant's argument in the Response filed November 16, 2004:

> The Applicant contends, "Schachner '730 neither discloses nor suggests predicting an error rate on the comparative basis of and input sequence and a corresponding output sequence."

The Examiner's rebuttal is broken down in parts A-C for clarity sake in the following:

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Part A

> The Examiner disagrees and asserts that the abstract in Schachner teaches that the circuit in Figure 14 of Schachner is a means for analyzing a signal using Data Comparator 1414 in Figure 14 to compare the input signal received after storage on the recording medium to a reference value representing the input value prior to storage

The Applicant expressly traverses the Examiner's assertion that Schachner in any way discloses comparing the input signal to a reference value representing the input value prior to storage. As discussed above, Schachner is wholly silent regarding comparing a particular input signal to a reference signal made from that particular input signal. This assertion is based on a misplaced reading of Schachner.

Part B

> (col. 21 lines 38-41 of Schachner explicitly teach that the first NRZ data input becomes the reference data suing [sic] SAM values to determine proximity (col. 16, lines 49-65 in Schachner; see also claims 50 and 51). Col. 4, lines 32-35 in Schachner explicitly suggests the use of SAM to determine error rate.

Piecemeal examination is to be avoided. *In re Blamer*, 1993 U.S. App. Lexis 24558 (1993); MPEP 707.07(g). Here the Examiner contrarily applies an improper piecemeal analysis by combining portions of alternative-embodiments of the Schachner disclosure. The first part of this assertion is part of Schachner's discussion in the NRZ Compare error method. However, the SAM value discussion (col. 16 and col. 4) is part of the Maximum Likelihood Distance error method. There is neither disclosure from Schachner, explicit or implicit, nor would a skilled artisan interpret Schachner to disclose that the NRZ method, which uses a comparative reference signal, would be combined with the SAM analysis, which does not use a comparative reference signal. There is also absolutely no disclosure

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motivating the skilled artisan to combine the alternative embodiments of Schachner to arrive at the embodiments of the present invention as claimed. This assertion is based on a misplaced reading of Schachner, and is irrelevant in relation to the claimed comparison of the input sequence and output sequence.

Part C

> Hence Schachner teaches predicting an error rate on the comparative basis of an input reference sequence and a corresponding output sequence of stored input values using SAM values.

With all due respect, the Examiner's conclusion is wholly incomprehensible. Schachner in fact discloses using the Maximum Likelihood Distance (ML Distance) method for determining the quality of the head signal. The output is sampled and passed through a Viterbi detector which selects the most likely sequence of bits. When a new bit is appended, the sequenced amplitude margin (SAM) is the difference between the mean squared distance of the selected sequence and the other possible sequence leading to the selected state. The SAM analysis is distinguishable from the comparative basis of the NRZ Compare method, because the SAM analysis performs the analysis without a reference signal. (see, for example, col. 16 line 66 to col. 17 line 10)

Accordingly, the Examiner's statement that Schachner discloses a comparative analysis by combining the NRZ method with SAM analysis is wholly misplaced, and ultimately irrelevant in view of the claimed comparison of input and output sequences.

Rejection Under 35 USC 102(e)

Claims 1-3, 15-20, and 27 were rejected as being anticipated by U.S. Patent No. 6,442,730 issued to Schachner ("Schachner '730"). This rejection is respectfully traversed.

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Claim 1

Schachner '730 cannot sustain the Section 102 rejection because it does not disclose all the features of claim 1, which recites at least the following:

> *an emulation circuit...which arranges the input data into an input sequence of multibit symbols each having a first selected symbol length and arranges the output data into an output sequence of multibit symbols each having the first selected length, wherein the emulation circuit determines a number of erroneous symbols in the output sequence in relation to differences between the input sequence and the output sequence....*
> (excerpt of claim 1, emphasis added)

The embodiments of the present invention as claimed in claim 1 cover a digital channel that both stores input data to a medium and subsequently retrieves output data that is associated with the input data from the medium. This claimed subject matter is supported in the specification in at least the following excerpts: "Referring now to FIG. 5, shown therein is a general block diagram of a readback circuit 135 useful in recovering the data encoded by FIG. 3." (page 9, lines 5-6); "FIG. 7 generally represents a readback circuit 165 used to recover the data encoded by FIG. 6." (page 11, lines 16-17).

Claim 1 further explicitly recites the emulation circuit arranging the input data into an input sequence and arranging the output data into an output sequence. Thus, the embodiments of the present invention as claimed in claim 1 determines the number of erroneous symbols, or predicted error rate performance, in relation to differences between the input sequence and the output sequence.

Schachner '730 contrarily analyzes an analog input signal from the data storage medium in relation to a reference signal. The reference signal is a benchmark providing expected values; see, for example, Schachner '730 col. 14 lines 49-51: "During use the user negotiates

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through the appropriate menus and stores a "good" reference analog waveform 310 and then inputs an input waveform 320 to be tested." Alternatively, the reference signal can be provided by a first NRZ data input signal. However, Schachner does not contemplate comparing the reference signal with the input signal used to make the reference signal.

Furthermore, Schachner '730 is inherently incapable of determining the error rate performance in accordance with embodiments of the present invention as claimed in claim 1 because it does not contemplate emulating the write channel whatsoever. See, for example: "Thus, this improved apparatus and method of the invention improve the user's ability to: Analyze PRML signals from the pre-amp through the output channel." (Schachner '730, col. 2 lines 32-33)

The Applicant expressly traverses the Examiner's following assertion in the Office Action: "Schachner teaches a reference signal is selected as an input sequence for comparing with readback (output) data to track errors...." This statement overreachingly reads the claimed comparison of the input sequence and output sequence of claim 1 onto Schachner '730's comparison of an input signal to an input reference value. See, for example, Schachner '730 claim 2 which recites "receiving a reference signal." Schachner '730 neither discloses nor suggests predicting an error rate on the comparative basis of an input sequence and a corresponding output sequence. The Examiner's construction of claim 1, forming the basis of the rejection, is erroneously too broad thereby denying the Applicant's rightful claimed subject matter.

Schachner '730 is silent regarding determining errors in relation to differences between the input sequence and the output sequence. Accordingly, the Section 102 rejection over Schachner '730 is erroneous as a matter of law because the cited reference does not disclose

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all the features recited by claim 1. Reconsideration and withdrawal of the present rejection of claim 1 and the claims depending therefrom are respectfully requested.

Claim 15

Schachner '730 cannot sustain the Section 102 rejection because it does not disclose all the features of claim 15, which recites at least the following:

> *comparing the output sequence with the input sequence to determine a first number of erroneous symbols in the output sequence.*
> (excerpt of claim 15, emphasis added)

As discussed above for claim 1, the embodiments of the present invention as claimed in claim 15 cover arranging input data into an input sequence and arranging the associated output data into an output sequence. The error performance is determined on the basis of comparing these input and output sequences.

As further discussed above for claim 1, Schachner '730 only compares two inputs and is inherently incapable of the claimed comparison because it contemplates emulating only the read channel, and not the write channel. Schachner '730 is silent regarding the claimed comparing the output sequence with the input sequence to determine a first number of erroneous symbols in the output sequence. Accordingly, the Section 102 rejection over Schachner '730 is erroneous as a matter of law because the cited reference does not disclose all the features recited by claim 15. Reconsideration and withdrawal of the present rejection of claim 15 and the claims depending therefrom are respectfully requested.

Rejection Under 35 USC (103)

Claims 4, 6, 8, 9, 11, 12, 23, 24, and 26 were rejected as being unpatentable over Schachner '730. Claims 5, 7, 10, 13, 14, 21, 22, and 25 were rejected as being unpatentable

over Schachner '730 in view of Reed '198. This rejection is traversed because these claims are allowable as dependent claims of an allowable independent claim, for reasons above, that provide additional limitations thereto. Reconsideration and withdrawal of the present rejection are respectfully requested.

Conclusion

This is a complete response to the Office Action mailed January 21, 2005. The Applicant respectfully requests that the Examiner reconsider the application and allow all of the pending claims. The Applicant has also filed herewith a request for telephone interview, the date and time of which is left to the Examiner's discretion as to determine some time after having reviewed this Response, and concluding there remain any claims not passed to allowance. The interview is necessary because, as understood, the Examiner has finally rejected the claims based on a misplaced reading of the cited reference, resulting in unduly delaying the issuance of valuable patent rights to which the Applicant is entitled. The Examiner is invited to contact the below signed Attorney should any questions arise concerning this response.

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